REMARKS

Claims 1-29 were rejected under 35 USC § 103(a) as being unpatentable over Drako et al. (U.S. 5,371,877) in view of Rust et al., (U.S. 5,699,530), in further view of DeWilde et al. (U.S. 6,434,674).

Drako discusses implementing a dual port FIFO memory by using two banks of single-port RAM, and an apparatus for interleaving reads and writes between banks such that successive writes will be to different memory banks, and such that the memory bank not being written may be read.

Rust describes a circular RAM-based FIFO buffer using interleaved storage and cross pointers. A first RAM bank stores even data, and a second RAM bank stores odd data. A read pointer and a write pointer use shift registers to select the written or read element.

DeWilde is relied upon to show a FIFO buffer 26 located between a memory-coupled MUX 12 and controllers 32 and 34. The FIFO units are described as bi-directional, but little additional detail is given.

The claims of the present invention as amended, in contrast, recite a system for controlling write access to banks in a dual-bank FIFO to ensure written data is valid, where the dual-bank FIFO serves as a buffer between a memory and a memory controller or memory controller interface. More specifically, the pending claims recite first and second ports for connecting the dual bank FIFO buffer between a memory and a memory controller (Claims 1 and 10), operation within a memory controller as a dual-bank FIFO connected between the data input and the memory and operable to buffer the read data (Claim 11), or coupling a dual-bank FIFO

between memory and a memory controller in a computerized information handling system (Claim 20).

These amended claims further recite first and second write pointers associated with first and second banks of memory elements, each pointer operable to allow received data to be written to the associated bank of memory when the other is in a null state, where the write pointer state is derived from received strobe signal preamble timing. Such pointers and functions are not found in the cited references.

Each of these claims therefore recites features including a structure or function including buffering data between a memory and a memory controller or memory controller data input, and further including a multiple write pointer structure and function, which distinguish the pending claims from combination of Drako, Rust, and DeWilde.

Further, because each of the references solves a problem other than that addressed by the claims of the present invention, and because none of the references teach or suggest combination with the other references to address the subject of buffering data between a dual-bank memory and a memory controller, combination of such reference is improper.

Because the cited references fail to teach the structure and function recited in the pending claims of buffering data between a memory and a memory controller or memory controller data input, and fail to disclose the write pointer structure or function recited in the pending claims, the pending claims are believed to be distinct from the cited references. Reversal of the rejection of the pending claims 1-29 is therefore respectfully requested

SUPPLEMENTAL AMENDMENT & RESPONSE UNDER 37 CFR 1.116
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Docket No: 499.078US1

Notice of Appeal

An Appeal Brief was filed in this matter on November 15, 2004. The Appeal Brief should be considered as formally withdrawn.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9581 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully Submitted,

MARK R. SIKKINK ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9581

Date __Feb 15 05__   By _____
John M. Dahl
Reg. No. 44,639